## **CLAIMS**

We claim:

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1. A method of forming a double gated SOI channel transistor, comprising the steps of:

providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI silicon oxide layer and an upper SOI silicon layer;

patterning the SOI silicon layer to form a patterned SOI silicon layer;

forming a dummy layer over the SOI silicon oxide layer and the patterned SOI silicon layer;

patterning the dummy layer to expose:

a portion of the lower SOI silicon oxide layer; and

a central portion of the patterned SOI silicon layer;

to form a damascene opening therein to define a source structure and a drain structure of the patterned SOI silicon layer;

patterning the exposed lower SOI silicon oxide layer to form a recess;

forming gate layer portions around the portion of the patterned SOI silicon layer exposed by the damascene opening;

forming a planarized layer portion within the damascene opening; the planarized layer portion including a bottom gate and a top gate; and

removing the patterned dummy layer to form the double gated SOI channel transistor.

2. The method of claim 1, wherein the structure is a semiconductor substrate.

- 3. The method of claim 1, wherein the structure is comprised of silicon or germanium.
- 4. The method of claim 1, wherein the SOI silicon layer has a thickness of from about 300 to 2000Å; the SOI silicon oxide layer has a thickness of from about 1000 to 5000Å; the dummy layer has a thickness of from about 1000 to 3000Å; and the gate layer portions each have a thickness of from about 5 to 200Å.
- 5. The method of claim 1, wherein the SOI silicon layer has a thickness of from about 500 to 1500Å; the SOI silicon oxide layer has a thickness of from about 2000 to 4000Å; the dummy layer has a thickness of from about 1500 to 2500Å; and the gate layer portions each have a thickness of from about 10 to 50Å.
- 6. The method of claim 1, wherein the dummy layer is comprised of nitride, silicon nitride or silicon oxynitride.
- 7. The method of claim 1, wherein the dummy layer is comprised of nitride.
- 8. The method of claim 1, wherein the exposed lower SOI silicon oxide layer is patterned from about 500 to 3000Å deep.
- 9. The method of claim 1, wherein the exposed lower SOI silicon oxide layer is patterned from about 1000 to 2000Å deep.
- 10. The method of claim 1, wherein the exposed lower SOI silicon oxide layer is patterned using an HF wet etch.

- 11. The method of claim 1, wherein the patterned lower SOI silicon oxide layer is undercut from about 500 to 3000Å underneath the portions of the twice patterned SOI silicon layer.
- 12. The method of claim 1, wherein the patterned lower SOI silicon oxide layer is undercut from about 1000 to 2000Å underneath the portions of the twice patterned SOI silicon layer.
- 13. The method of claim 1, wherein the gate layer is:

oxide or silicon oxide formed by a furnace oxidation process or a rapid thermal processing process; or

- a dielectric material having a dielectric constant of greater than about 3.0 formed by a chemical vapor deposition method.
- 14. The method of claim 1, wherein the gate layer is:

oxide or silicon oxide formed by a furnace oxidation process or a rapid thermal processing process; or

- a dielectric material such as  $HSi_xO_2$  or  $ZrO_2$  having a dielectric constant of greater than about 3.0 formed by a chemical vapor deposition method.
- 15. The method of claim 1, wherein the gate layer is oxide formed by a rapid thermal processing process.
- 16. The method of claim 1, wherein the planarized layer portion is comprised of polysilicon, tungsten, W-Si<sub>x</sub> or aluminum.

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- 17. The method of claim 1, wherein the planarized layer portion is comprised of polysilicon.
- 18. The method of claim 1, including the step of doping the source structure and a drain structure after removal of the patterned dummy layer.
- 19. The method of claim 1, wherein the central exposed portion of the patterned SOI silicon layer has surfaces that are smooth.
- 20. A method of forming a double gated SOI channel transistor, comprising the steps of:

providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI silicon oxide layer and an upper SOI silicon layer;

patterning the SOI silicon layer to form a patterned SOI silicon layer;

forming a dummy layer over the SOI silicon oxide layer and the patterned SOI silicon layer;

patterning the dummy layer to expose:

- i) a portion of the lower SOI silicon oxide layer; and
- ii) a central portion of the patterned SOI silicon layer; to form a damascene opening therein to define a source structure and a drain structure of the patterned SOI silicon layer;

patterning the exposed lower SOI silicon oxide layer to form a recess; forming gate layer portions around the portion of the patterned SOI silicon

layer exposed by the damascene opening; the gate layer being comprised of:

- i) oxide or silicon oxide formed by a furnace oxidation process or a rapid thermal processing process; or
- ii) a dielectric material such as HSi<sub>x</sub>O<sub>2</sub> or ZrO<sub>2</sub> having a dielectric constant of greater than about 3.0 formed by a chemical vapor deposition method;

forming a planarized layer portion within the damascene opening; the planarized layer portion including a bottom gate and a top gate; and

removing the patterned dummy layer to form the double gated SOI channel transistor.

- 21. The method of claim 20, wherein the structure is a semiconductor substrate.
- 22. The method of claim 20, wherein the structure is comprised of silicon or germanium.
- 23. The method of claim 20, wherein the SOI silicon layer has a thickness of from about 300 to 2000Å; the SOI silicon oxide layer has a thickness of from about 1000 to 5000Å; the dummy layer has a thickness of from about 1000 to 3000Å; and the gate layer portions each have a thickness of from about 5 to 200Å.
- 24. The method of claim 20, wherein the SOI silicon layer has a thickness of from about 500 to 1500Å; the SOI silicon oxide layer has a thickness of from about 2000 to 4000Å; the dummy layer has a thickness of from about 1500 to 2500Å; and the gate layer portions each have a thickness of from about 10 to 50Å.

- 25. The method of claim 20, wherein the dummy layer is comprised of nitride, silicon nitride or silicon oxynitride.
- 26. The method of claim 20, wherein the dummy layer is comprised of nitride.
- 27. The method of claim 20, wherein the exposed lower SOI silicon oxide layer is patterned from about 500 to 3000Å deep.
- 28. The method of claim 20, wherein the exposed lower SOI silicon oxide layer is patterned from about 1000 to 2000Å deep.
- 29. The method of claim 20, wherein the exposed lower SOI silicon oxide layer is patterned using an HF wet etch.
- 30. The method of claim 20, wherein the patterned lower SOI silicon oxide layer is undercut from about 500 to 3000Å underneath the portions of the twice patterned SOI silicon layer.
- 31. The method of claim 20, wherein the patterned lower SOI silicon oxide layer is undercut from about 1000 to 2000Å underneath the portions of the twice patterned SOI silicon layer.
- 32. The method of claim 20, wherein the gate layer is oxide formed by a rapid thermal processing process.

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- 33. The method of claim 20, wherein the planarized layer portion is comprised of polysilicon, tungsten, W-Si<sub>x</sub> or aluminum.
- 34. The method of claim 20, wherein the planarized layer portion is comprised of polysilicon.
- 35. The method of claim 20, including the step of doping the source structure and a drain structure after removal of the patterned dummy layer.
- 36. The method of claim 20, wherein the central exposed portion of the patterned SOI silicon layer has surfaces that are smooth.
- 37. A method of forming a double gated SOI channel transistor, comprising the steps of:

providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI silicon oxide layer and an upper SOI silicon layer;

patterning the SOI silicon layer to form a patterned SOI silicon layer;

forming a dummy layer over the SOI silicon oxide layer and the patterned SOI silicon layer; the dummy layer being comprised of nitride, silicon nitride or silicon oxynitride;

patterning the dummy layer to expose:

- i) a portion of the lower SOI silicon oxide layer; and
- ii) a central portion of the patterned SOI silicon layer; to form a damascene opening therein to define a source structure and a drain structure of the patterned SOI silicon layer;

patterning the exposed lower SOI silicon oxide layer to form a recess;

forming gate layer portions around the portion of the patterned SOI silicon layer exposed by the damascene opening; the gate layer being comprised of:

- i) oxide or silicon oxide formed by a furnace oxidation process or a rapid thermal processing process; or
- ii) a dielectric material such as HSi<sub>x</sub>O<sub>2</sub> or ZrO<sub>2</sub> having a dielectric constant of greater than about 3.0 formed by a chemical vapor deposition method;

forming a planarized layer portion within the damascene opening; the planarized layer portion including a bottom gate and a top gate; and

removing the patterned dummy layer to form the double gated SOI channel transistor.

- 38. The method of claim 37, wherein the structure is a semiconductor substrate.
- 39. The method of claim 37, wherein the structure is comprised of silicon or germanium.
- 40. The method of claim 37, wherein the SOI silicon layer has a thickness of from about 300 to 2000Å; the SOI silicon oxide layer has a thickness of from about 1000 to 5000Å; the dummy layer has a thickness of from about 1000 to 3000Å; and the gate layer portions each have a thickness of from about 5 to 200Å.
- 41. The method of claim 37, wherein the SOI silicon layer has a thickness of from about 500 to 1500Å; the SOI silicon oxide layer has a thickness of from about 2000 to 4000Å; the dummy layer has a thickness of from about 1500 to 2500Å; and the gate layer portions each have a thickness of from about 10 to 50Å.

- 42. The method of claim 37, wherein the dummy layer is comprised of nitride.
- 43. The method of claim 37, wherein the exposed lower SOI silicon oxide layer is patterned from about 500 to 3000Å deep.
- 44. The method of claim 37, wherein the exposed lower SOI silicon oxide layer is patterned from about 1000 to 2000Å deep.
- 45. The method of claim 37, wherein the exposed lower SOI silicon oxide layer is patterned using an HF wet etch.
- 46. The method of claim 37, wherein the patterned lower SOI silicon oxide layer is undercut from about 500 to 3000Å underneath the portions of the twice patterned SOI silicon layer.
- 47. The method of claim 37, wherein the patterned lower SOI silicon oxide layer is undercut from about 1000 to 2000Å underneath the portions of the twice patterned SOI silicon layer.
- 48. The method of claim 37, wherein the gate layer is oxide formed by a rapid thermal processing process.
- 49. The method of claim 37, wherein the planarized layer portion is comprised of polysilicon, tungsten, W-Si<sub>x</sub> or aluminum.

- 50. The method of claim 37, wherein the planarized layer portion is comprised of polysilicon.
- 51. The method of claim 37, including the step of doping the source structure and a drain structure after removal of the patterned dummy layer.
- 52. The method of claim 37, wherein the central exposed portion of the patterned SOI silicon layer has surfaces that are smooth.